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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/629,581 | 07/30/2003 | Sin-Gu Kang | 6192.0143.D1 | 6203 |

7590 11/29/2005

McGuireWoods LLP
Suite 1800
1750 Tysons Boulevard
McLean, VA 22102

| EXAMINER | |
|---|---|
| CHOW, DOON Y | |
| **ART UNIT** | **PAPER NUMBER** |
| 2677 | |

DATE MAILED: 11/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/629,581 | KANG, SIN-GU | |
| | Examiner | Art Unit | |
| | Dennis-Doon Chow | 2677 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *18 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *23-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *23-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Double Patenting*

1. Claims 23-30 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-22 of U.S. Patent No. 6,621,547. Although the conflicting claims are not identical, they are not patentably distinct from each other because they claim a similar invention with different wordings.

For example:

| Claim 23 of the present claims. | Claims 1 and 4 of the patented claims |
|---|---|
| 23. A module for determining a driving signal timing for a liquid crystal display (LCD) device, comprising:<br>a flexible base substrate;<br>a gate-driving signal input line formed on one side of the base substrate that applies a gate-driving signal to the gate-driving signal input line;<br>a gate-driving IC mounted on the flexible base substrate to be connected to the gate-driving signal input line; and<br>a plurality of gate-driving signal output lines formed on the flexible base substrate that are connected to output terminals of the gate driving IC, the plurality of gate-driving signal output lines adapted to allow the gate-driving signal outputted from the output terminals of the gate-driving IC to have a linear level and to be applied to the plurality of gate lines, wherein the gate driving IC linearly modifies a level of the gate-driving signal inputted to a first gate line through a last gate line of a plurality of gate lines formed on a TFT substrate when diverging the applied gate-driving signal in a parallel way so as to input the applied gate-driving signal to the plurality of gate lines, and then, output the linearly modified gate-driving signal through output terminals thereof, and<br>wherein a signal transmitting line is formed on the flexible base substrate and connected<br>to the gate-driving signal input line in parallel, so that the gate-driving signal applied to the gate-driving signal input line is not applied to the gate-driving IC and is bypassed toward outside of the flexible base substrate. | 1. A module for determining a driving signal timing for a liquid crystal display (LCD) device, comprising:<br>a flexible base substrate;<br>a gate-driving signal input line formed on one side of the base substrate so that a gate-driving signal is applied to the gate-driving signal input line;<br>a gate-driving IC mounted on the base substrate to be connected to the gate-driving signal input line, the gate driving IC adapted to modify linearly a level of the gate-driving signal inputted to a first gate line through a last gate line of a plurality of gate lines formed on a TFT substrate when allowing the applied gate-driving signal to be diverged in a parallel way so as to input it to the plurality of gate lines, and then, output the linearly modified gate-driving signal through output terminals thereof; and<br>a plurality of gate-driving signal output lines formed on the base substrate in such a manner that the plurality of gate-driving signal output lines are connected to output terminals of the gate driving IC, the plurality of gate-driving signal output lines adapted to allow the gate-driving signal outputted from the output terminals of the gate-driving IC to have a linear level and to be applied to the plurality of gate lines.<br><br>4. The module according to claim 1, wherein a signal transmitting line is formed on the base substrate of the gate-driving IC in such a manner that the signal transmitting line is connected to the gate-driving signal input line in parallel, so that the gate-driving signal applied to the gate-driving |

| | |
|---|---|
| | signal input line is not applied to the gate-driving IC and is bypassed to output it to the outside of the base substrate. |

***Allowable Subject Matter***

2. Claims 23-30 are allowed.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis-Doon Chow whose telephone number is 571-272-7767. The examiner can normally be reached on 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on 571-272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DENNIS-DOON CHOW
PRIMARY EXAMINER

Dennis-Doon Chow
Primary Examiner
Art Unit 2677

D. Chow